Flexible and Printed Electronics

LETTER

Influence of bank geometry on the electrical characteristics of printed organic field-effect transistors

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RECEIVED
17 July 2019

REVISED
25 September 2019

ACCEPTED FOR PUBLICATION
12 November 2019

PUBLISHED
25 November 2019

Keywords: printed electronics, organic field-effect transistors, uniformity, bank, crystallinity

Supplementary material for this article is available online

Abstract

The electrical characteristics of organic field-effect transistors (OFETs) based on small-molecule organic semiconductors (OSCs) have been significantly improved by employing various fabrication techniques in solution processes to enhance the OSC crystallinity. However, complicated fabrication and inhomogeneity of OFETs remain as challenges before commercialization. In this work, we have efficiently controlled the size and orientation of 6,13-bis(triisopropylsilylethynyl)-pentacene (TIPS-pentacene) crystalline domains by tuning the Cytop bank dimension, in which OSC inks are printed, to improve the device performance. The optimized bank pattern forms uniform thin film morphology and well-aligned TIPS-pentacene crystalline domains along the charge transport direction, resulting in four-fold increase in field-effect mobility and one third reduction in relative standard deviation.

1. Introduction

Organic field-effect transistors (OFETs) are of great interest in research and industry for the realization of flexible electronic devices due to their low-cost manufacturing, mechanical flexibility, lightweight and large-area processability. In particular, solution processes such as spin-coating [1], casting [2, 3], shearing [4, 5], and printing are strongly desired to fully exploit the advantages of OFETs [6, 7]. Among them, printing is considered as a promising candidate due to additive process, maskless patterning, and low waste. The electrical performance of printed devices has been remarkably enhanced by adopting new device structures [8, 9], optimizing printing processes [10], and improving crystallinity of the organic semiconductor (OSC) layers for the realization of practical electronic applications [11, 12]. In addition, the uniformity of OFETs has been improved by blending polymer insulators [13–15], tuning surface conditions [16], and reducing fabrication factors [17].

There have been many successful attempts with solution-processable 6,13-bis(triisopropylsilylethynyl)-pentacene (TIPS-pentacene) as the active channel material in OFETs. TIPS-pentacene, one of the most widely used small-molecule OSCs, has been successfully reported for high uniformity and field-effect mobility (μ_{FET}) by tuning the crystallinity, crystal orientation, and molecular packing of OSC thin films. The higher mobility is generally achieved when the OSC crystals are larger and well aligned along the direction of charge transport by controlling the direction and degree of crystallization over a device area [18, 19]. Yang *et al* reported a pneumatic nozzle printing technique to control the crystal growth of TIPS-pentacene thin films [10]. They controlled the size and orientation of crystalline domain by tuning the substrate temperature and printing speed. Bao and

coworkers have achieved patterned and aligned single-crystalline TIPS-pentacene thin films while maintaining non-equilibrium molecular packing motifs by fluid flow engineering [18]. They also demonstrated the growth of strained lattice and aligned crystals of TIPS-pentacene thin films by laterally confining the OSC crystal growth during solution shearing [19]. By combining the surface wetting properties and solution shearing, TIPS-pentacene crystalline domains were effectively patterned and aligned in a single step [20]. Xiao *et al* conveniently patterned TIPS-pentacene single-crystalline arrays by combining the space-restricted and field/force-induced strategies [21]. However, most of these techniques require complicated processes and specialized fabrication due to extra steps such as photolithography processes and/or selective surface treatments.

In this work, we introduce a simple strategy that efficiently improved the device performance and uniformity by using a pneumatic nozzle printing technique. The banks of Cytop were used to concentrate the OSC ink into defined areas by forming microwells, resulting in a uniform film morphology. We control the crystal size and crystalline domain orientation of TIPS-pentacene thin films by modifying the bank dimension in which OSC inks are printed. The electrical characteristics of OFETs, including uniformity, with various bank geometries were measured to investigate the effect of TIPS-pentacene thin film crystalline domain sizes and directions on the device performance. The morphology of TIPS-pentacene thin films was evaluated by determining the orientation and degree of crystalline domains. The OFET with the optimized bank geometry, resulting in well-aligned crystalline domains along the charge transport direction, exhibited a field-effect mobility of 0.23 $cm^2 V^{-1} s^{-1}$ and a relative standard deviation (RSD) of 16%, which was four-fold increase and one third decrease, respectively, compared with other bank geometries. This work provides a step forward to develop practical electronic applications with high device performance and uniformity while maintaining an easy and simple fabrication process.

2. Experimental

2.1. Device fabrication

A bottom-gate top-contact OFET was fabricated on a glass substrate (Eagle XG, Corning). A 40 nm thick aluminum (Al) gate electrode was thermally evaporated through a shadow mask on the substrate. The 200 nm thick copolymerized thin film of poly-para-xylylene (Parylene) C (diX-C, Daisankasei Co., Ltd) and Parylene F (VT4, Suzhou Chireach Biomedical Technology Co., Ltd) was simultaneously deposited for the gate dielectric at a weight ratio of 0.7:0.3. The fabrication process and condition for the copolymerized Parylene gate dielectric can be found in detail in our previous study [22]. For the printing of banks in which OSC inks are printed, Cytop (CTL-809M, Asahi Glass) was dissolved in a fluorinated solvent (CT-Solv.180, Asahi Glass) at a volume ratio of 1:2. The bank solution was printed using a pneumatic nozzle printer (350PC, Musashi Engineering, Inc.) on glass substrates, followed by thermal annealing treatment at 100 °C for 10 min on a hotplate to remove residual solvents. The substrate and nozzle temperatures were maintained at 40 °C during the dispenser patterning process. The OSC solution was prepared with a blend of 2.5 mg ml^{-1} TIPS-pentacene (>99.9%, Ossila) and 1.25 mg ml^{-1} polystyrene (PS) (MW ~ 280 000, Sigma-Aldrich) dissolved in mesitylene (98%, Sigma-Aldrich). The OSC solution was printed onto the area defined by the banks using the dispenser, followed by thermal annealing treatment at 70 °C for 10 min on a hotplate for crystallization of the TIPS-pentacene thin film and removal of residual solvent. The temperatures of the substrate and nozzle were maintained at 30 °C during the printing process. Finally, a 40 nm thick silver (Ag) was thermally evaporated through a shadow mask for the source and drain electrodes. Their channel width and length are 1000 and 50 μm, respectively. The metal–insulator–metal (MIM) capacitor was fabricated by sandwiching the Parylene thin film between two Al electrodes.

2.2. Characterization

The thickness of the thin films was measured by a stylus surface profiler (DektakXT, Bruker). The capacitance of the MIM capacitors was measured using an LCR meter (ZM2376, NF Corporation) within the frequency range of 1 Hz to 1 MHz. The electrical characteristics of OFETs were measured using a semiconductor parameter analyzer (4200-SCS, Keithley) under ambient conditions inside a dark box. The two-dimensional grazing incidence x-ray diffraction (2D-GIXRD) analysis was carried out at the 3C beamline ($\lambda = 1.37$ Å) of the Pohang Acceleration Laboratory in Korea. The crystalline orientation of TIPS-pentacene thin films was recorded by polarized optical microscope (POM) (DM2700M, Leica).

3. Results and discussion

Figure 1(a) illustrates the fabrication processes for the printed OFET based on TIPS-pentacene (see supplementary movies 1 and 2 is available online at stacks.iop.org/FPE/4/042001/mmedia). After the deposition of the gate electrode and dielectric layers, Cytop solution was printed on the gate dielectric using a pneumatic nozzle printer to form the bank patterns, followed by the OSC solution printing in the defined area by bank patterns. The Cytop banks were hydrophobic, whereas the inner surface was hydrophilic, to prevent droplets pinning at the bank walls and ensure that the TIPS-pentacene inks were filled uniformly

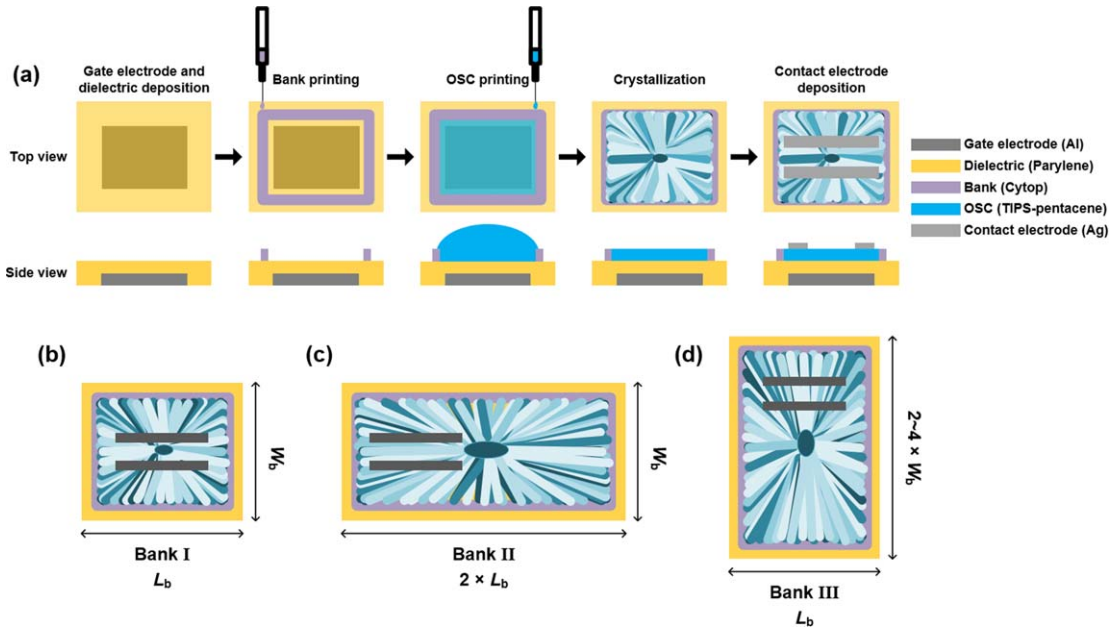

Figure 1. Schematic illustrations of (a) the fabrication processes for printed OFET and (b)–(d) TIPS-pentacene thin film morphologies printed into bank (b) I, (c) II, and (d) III patterns. The bank length (L_b) and bank width (W_b) are 1830 μm and 1120 μm, respectively.

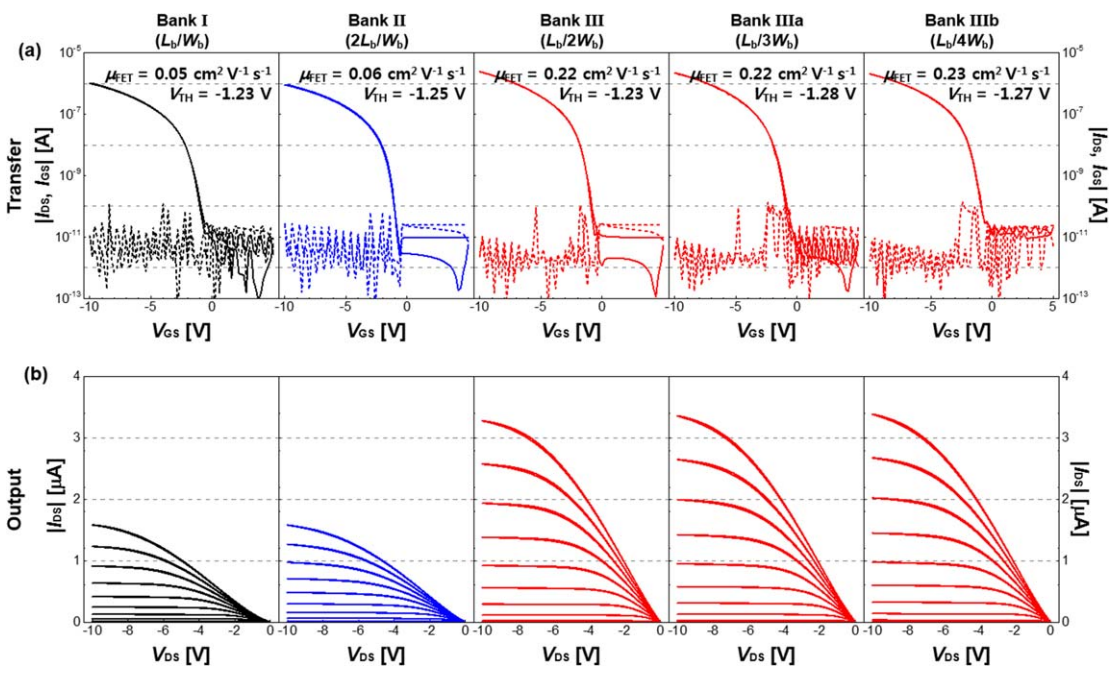

Figure 2. Typical (a) transfer and (b) output curves for TIPS-pentacene-based OFETs with bank I (black lines), bank II (blue lines), and bank III (red lines). The solid and dashed lines represent I_{DS} and I_{GS}, respectively.

and evaporated slowly. To control the crystalline domains of the TIPS-pentacene thin films, we fabricated bank patterns in three different dimensions; the length and width of banks I, II, and III were 1830 μm × 1120 μm, 3660 μm × 1120 μm, and 1830 μm × 2240 μm, respectively (figures 1(b)–(d) and S1). Bank I, the reference pattern herein, was the most desired dimension because it requires the smallest occupied area and least material consumption. A TIPS-pentacene thin film printed in bank I shows a radial crystalline domain as shown in figure S2(a). Under bank II, the extended length pattern, the crystalline domains of TIPS-pentacene thin films were more aligned in a parallel manner with respect to the bank I pattern, which were perpendicular to the charge transport direction (figure S2(b)). Meanwhile, more perpendicularly aligned crystalline domains of TIPS-pentacene thin films with respect to the bank I pattern were observed under bank III, the extended width pattern (figure S2(c)).

Table 1. Electrical parameters of printed OFETs under banks I, II, and III patterns.

Bank pattern	V_{TH} (V)	I_{on}/I_{off} ($\times 10^5$)	μ_{FET} ($cm^2\ V^{-1}\ s^{-1}$)	RSD (%)
Bank I	-1.23 ± 0.14	0.94 ± 0.91	0.05 ± 0.03	50.28
Bank II	-1.25 ± 0.06	0.87 ± 0.14	0.06 ± 0.02	32.08
Bank III	-1.23 ± 0.04	1.51 ± 0.61	0.22 ± 0.04	16.68
Bank IIIa	-1.28 ± 0.05	3.65 ± 1.78	0.22 ± 0.04	18.07
Bank IIIb	-1.27 ± 0.05	2.97 ± 1.09	0.23 ± 0.04	16.12

*Averaged over 20 devices.

*The RSD was calculated considering the fourth decimal point.

$$* \text{ RSD} = \frac{\text{variation } (\mu_{FET})}{\text{average } (\mu_{FET})} \times 100\%.$$

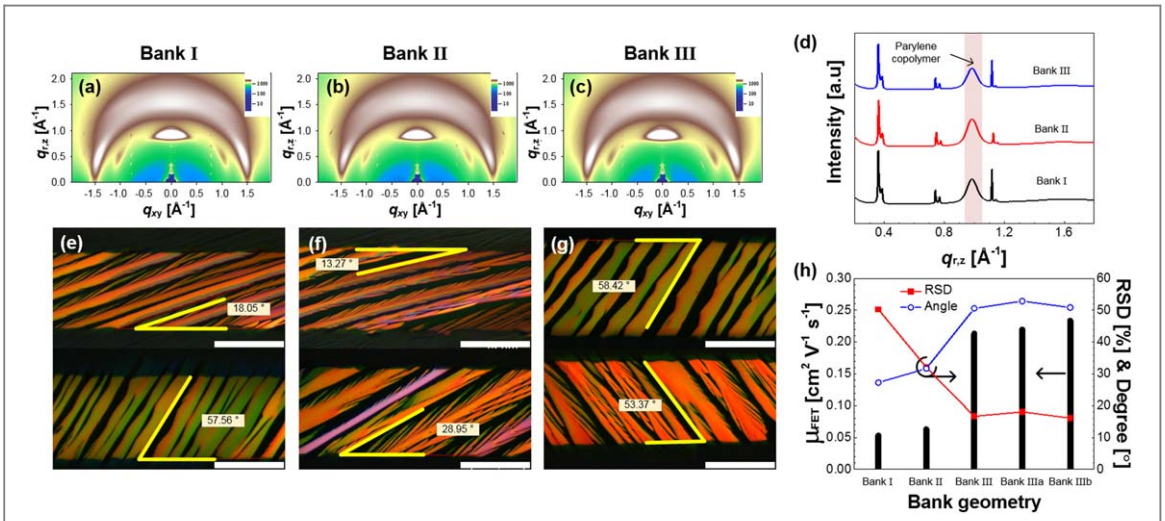

Figure 3. (a)–(c) 2D-GIXRD patterns of TIPS-pentacene thin films printed in bank (a) I, (b) II, and (c) III patterns. (d) Out-of-plane XRD patterns of TIPS-pentacene thin films under various bank patterns. (e)–(g) POM images of TIPS-pentacene thin films printed in bank (e) I, (f) II, and (g) III patterns. The scale bar represents 30 μm. (h) Field-effect mobility (red solid symbols), relative standard deviation (blue open symbols), and crystalline domain degree (black bars) of OFETs under various bank patterns.

The electrical characteristics were measured to investigate the effects of bank patterns on the device performance (figure 2). To verify only the effects of bank patterns, we deposited the gate dielectric and OSC layers at the same time. The transfer characteristics represented in terms of the drain-source current (I_{DS}) as a function of the gate-source voltage (V_{GS}) were considerably dependent on the bank types (figure 2(a)). The OFET under bank III exhibited two times higher I_{DS} than that under banks I and II. However, the gate-source current (I_{GS}) was measured in the range of 10^{-12} to 10^{-10} A due to the reliable Parylene copolymer gate dielectric bulk quality [22]. The transfer curves show a negligible hysteresis behavior within the forward and reverse V_{GS} scans, regardless of bank patterns. To quantitatively compare the device performance, the electrical parameters such as threshold voltage (V_{TH}), μ_{FET}, and on/off current ratio (I_{on}/I_{off}) were extracted using the following equation:

$$I_{DS} = \frac{W_{CH}}{2L_{CH}} \mu_{FET} C_{OX} (V_{GS} - V_{TH})^2,$$

where C_{OX} is the gate dielectric capacitance per unit area and W_{CH} and L_{CH} are the channel width and length, respectively. The extracted dielectric constant and estimated dielectric thickness were 3.15 at 10 Hz and 200 nm, respectively (figure S3). The extracted V_{TH} was about -1.24 V, regardless of bank type, because the same device structure was employed for the fabrication of OFETs. On the other hand, other parameters such as μ_{FET} and I_{on}/I_{off} varied slightly with the bank patterns. The OFET under bank III exhibited the highest μ_{FET} of 0.22 $cm^2\ V^{-1}\ s^{-1}$ compared to those under banks I and II, which showed μ_{FET} values of 0.05 and 0.06 $cm^2\ V^{-1}\ s^{-1}$, respectively. An I_{on}/I_{off} higher than 10^5 was obtained from the OFET under bank III while OFETs under banks I and II showed a half order of magnitude decrease of I_{on}/I_{off}. To optimize the bank dimensions, we further extended the bank width by four times, namely banks IIIa and IIIb. Despite longer length of the bank patterns, OFETs show negligible changes in terms of the V_{TH}, μ_{FET}, and I_{on}/I_{off} compared to bank III. The output characteristics supported the observations that the device performance was considerably dependent on the bank patterns (figure 2(b)). The output curves show good saturation behaviors and no sign of significant contact resistance issues, regardless of bank type. The results indicated that bank III improves the device performance, resulting in four times enhancement of μ_{FET} and two times higher I_{on}/I_{off}, without

Table 2. Comparison of fundamental parameters of OFETs based on TIPS-pentacene.

Author [reference]	OSC deposition method/Number of extra process for OSC	OSC condition	Operation voltage[V_{GS}/V_{DS}]	L_{CH}/W_{CH}	μ_{FET} ($cm^2\ V^{-1}\ s^{-1}$)	RSD (%)
Yang *et al* [10]	Pneumatic printing/0	16 mg ml^{-1}	−50/−100	100/300	0.5	~40
Raghuwanshi *et al* [12]	Drop casting/1	0.5 wt%	−10/−10	153/973	0.44 ± 0.25	56.8
Bharti *et al* [3]	Drop casting/0	0.5 wt%	−5/−5	278/250	0.5 ± 0.3	60
Kim *et al* [5]	Solution shearing/5	2 mg ml^{-1}	−100/−100	40/400	2.26 ± 0.6	27
Diao *et al* [18]	Solution shearing/6	16 mg ml^{-1}	−100/−100	50/1000	8.2 ± 1.2	14.7
Giri *et al* [19]	Solution shearing/5	16 mg ml^{-1}	−40/−40	5/2	1.12 ± 0.23	21
Park *et al* [20]	Solution shearing/4	16 mg ml^{-1}	−50/−50	2/500	0.167	28
Xiao *et al* [21]	Solution shearing/1	8 mg ml^{-1}	−100/−100	30/240	~6.22	26
Kwak *et al* [7]	Inkjet printing/4	1 wt%	−40/−40	30/300	0.1 ± 0.03	30
This work	Pneumatic printing/1	2.5 mg ml^{-1}	−10/−10	50/1000	0.22 ± 0.04	16

additional fabrication processes for OSC deposition such as contact and interfacial engineering. The electrical parameters are summarized in table 1.

From the electrical results, we observed the correlation between TIPS-pentacene thin film crystalline degree and device performance (figure 3). The 2D-GIXRD analysis provided that the crystal structure of the TIPS-pentacene thin film was identical, regardless of bank pattern (figures 3(a)–(c)). The diffraction spectra under different bank patterns show (00*l*) reflections corresponding to a q_z axis with an interlayer distance (d-spacing, $d = 2\pi q_{r,z}^{-1}$) of 17.1 Å, which indicated that the molecular structure was perpendicular to the substrate (figure 3(d)). It is noted that the charge transport was hindered by the coexistence of the two different crystalline phases of small-molecule OSCs, inducing the charge carrier trap sites [23, 24]. The crystalline degree of the TIPS-pentacene thin films along to charge transport direction was determined using POM images (figures 3(e)–(g)). The crystalline domains show radial, parallel, and perpendicular respect to the charge transport direction under banks I, II, and III, respectively. Figure S4 and table S1 show a method for estimating the crystalline degree of TIPS-pentacene thin films from a POM images. The crystalline degree was averaged from ten channels for each bank pattern and summarized in table S2. Under bank III, the TIPS-pentacene thin film exhibited the highest crystalline degree of 51° (figure 3(h)). In addition, the crystalline degree was maintained for the extended width bank pattern. In contrast, the 27° and 32° of the crystalline domains were observed under banks I and II, respectively. This can be attributed to drying solvents from the center radially outward bank patterns.

The uniformity, one of the most important issues before commercialization, was determined by calculating the RSD of μ_{FET}. Despite a similar crystalline degree, the TIPS-pentacene thin film printed in bank I showed various crystalline degrees, resulting in high RSD of field-effect mobility. Under bank II, the crystalline domains of the TIPS-pentacene thin film were grown in a perpendicular direction respect to the charge transport, but larger and similar degrees of crystalline domains led to relatively low RSD compared to the OFET using bank I. The results indicated that bank III led to a higher and more oriented crystalline domain along the charge transport direction, which allows the isotropy of charge transport. The RSD was remarkably decreased from 50% to 16% by employing bank III. In other words, the crystalline domain in the same direction of the charge transport improves the uniformity and device performance simultaneously by reducing the trap states at the grain boundaries. The difference in field-effect mobility under different bank dimensions can be attributed to the difference in the degree of crystallinity of TIPS-pentacene thin films. In addition, bank III contains a lower density of grain boundaries, resulting in higher field-effect mobility. Furthermore, since the crystalline domains are aligned along the charge transport, field-effect mobility is likely further enhanced. Therefore, we concluded that the crystalline degree of TIPS-pentacene respect to the contact electrodes is the major factor that bring the higher device performance.

The fundamental parameters of OFETs based on TIPS-pentacene fabricated in various techniques were summarized in table 2 in terms of the number of extra processes for OSC deposition, OSC preparation, operation voltage, channel dimensions, field-effect mobility in the saturation regime, and RSD. We efficiently improved the device performance using only bank printing without complicated manufacturing processes. By comparing with previously published papers, the 0.22 $cm^2 V^{-1} s^{-1}$ of field-effect mobility is comparable or relatively low, but the operating voltage is only 10 V, and the RSD decreased to only 16%.

4. Conclusion

In conclusion, we have efficiently improved the device performance using a simple printing process, which added only one more step for OSC deposition. By tuning the bank pattern, we were able to control the degree of crystalline domains of TIPS-pentacene thin films. Under the optimized bank dimension, bank III, a TIPS-pentacene thin film exhibits a well-oriented crystalline domain along the charge transport direction, resulting in the highest μ_{FET} of 0.22 $cm^2 V^{-1} s^{-1}$ and lowest RSD of 16%, compared to OFETs using banks I and II. We observed the correlation between the degree of crystalline domains and device performance including the field-effect mobility and uniformity. Since the device structure and materials for OFETs were exactly the same, other parameters such as V_{TH}, contact resistance, and crystal structure of OSCs were almost identical, regardless of bank patterns. As a result, a solution-processed low-voltage OFET was successfully demonstrated in printing techniques and the device performance was considerably enhanced by tuning the bank dimensions, resulting of charge transport enhancement. This work provides an approach to the development of practical electronic devices in simple and low-cost manufacturing systems with high uniformity.

Acknowledgments

This work was supported by grants (Code No. CASE-2016R1E1A2020535 and CASE-2015M3A6A5065315) from the Center for Advanced Soft Electronics under the Global Frontier Research Program of the Ministry of Science and ICT of South Korea, and by the IT Consilience Creative Program (IITP-2019-R0346-15-1007) supervised by IITP (Institute for Information & Communications Technology Promotion).

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