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Active Charge Equalizer of Li-Ion Battery Cells Using Double Energy Carriers

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Received: 1 May 2019; Accepted: 12 June 2019; Published: 15 June 2019

Abstract: In this work, a new active balancing circuit is proposed. This circuit consists of a cell-access network and an energy-transfer network. The cell-access network requires $2n + 6$ switches, where n is the number of cells, and creates an energy-transfer path between unbalanced cells and the energy-transfer network. The energy-transfer network has double energy carriers and simultaneously implements cell-to-pack and pack-to-cell balancing operations without overlapping. As a result, a high power rate and fast balancing operation can be achieved by using two energy carriers in a single balancing circuit. The prototype of a proposed balancing circuit was built for six cells and then tested under various conditions; all cells in the state of charge (SOC) region of 70% to 80% were equalized after 93 min, and one charging/discharging period in the SOC region of 10% to 90% was increased by 8.58% compared to the non-balancing operation. These results show that the proposed circuit is a good way to balance charges among batteries in a battery pack.

Keywords: lithium-ion battery; charge equalizer; cell balancing circuit; battery management system

1. Introduction

In recent years, rechargeable batteries have been widely used in many applications, including energy storage systems (ESS), electric vehicles (EV), and photo voltaic (PV) systems. Among these, lithium-ion batteries (LIBs) in particular have high power density, high energy density, and a long life cycle [1,2], meaning they are widely used to store energy. However, a single LIB cell has a low voltage and low capacity, so LIB packs are fabricated by connecting the cells in series and in parallel. However, manufacturing is inconsistent and usage environments differ [3,4], causing voltage and capacity to differ among cells in a battery string. This variability means that all serially connected cells cannot be simultaneously charged or discharged within the safe operating area (SOA), which is the region between charging voltage limit (CVL) and discharging voltage limit (DVL) (Figure 1); the total capacity of the battery pack is determined by the strongest or weakest cell [5]. Therefore, the battery pack requires a balancing circuit which evens the capacities of the batteries [6–26].

Balancing circuits can be classified into passive type and active type. A passive balancing circuit dissipates the excessive energy of cells by using only shunt resistors, so the method is inexpensive and easy to control. However, the shunt resistor undergoes thermal heating, which can damage the battery pack, and the need to avoid this damage constrains the speed and energy-efficiency of the balancing operation [6,7]. In contrast, an active balancing circuit transfers the excess energy from the strong cells to the weak ones, making it a fast and energy-efficient way to balance the batteries [8–26].

Many types of active balancing circuits have been reported; these transfer the charge from cell to pack [8,9], from pack to cell [10–12], or from cell to cell [13–20]. Cell-to-pack balancing circuits are appropriate to balance strong cells during charging. Pack-to-cell balancing circuits are appropriate to balance weak cells during discharging. Cell-to-cell balancing circuits can balance battery cells

during both charging and discharging, but most circuits of this type can only transfer the charge between adjacent cells [13–16]; i.e., the balancing energy may be delivered through irrelevant cells. This extended routing limits the power-transfer efficiency and increases the time required to achieve balance. Some active balancing circuits such as those of the bidirectional flyback type [17], LC resonant type [18,19] and buck-boost type [20] can directly transfer energy between any cells in a battery string. However, these active balancing circuits have limited balancing power and speed and they may not be able to balance all batteries in high-voltage applications. To solve these problems, modularized and multi-layer equalizers have been introduced [21–26]. These can achieve a high balancing power rate and a short balancing time but need many active components, complex control algorithms, and a high computational load.

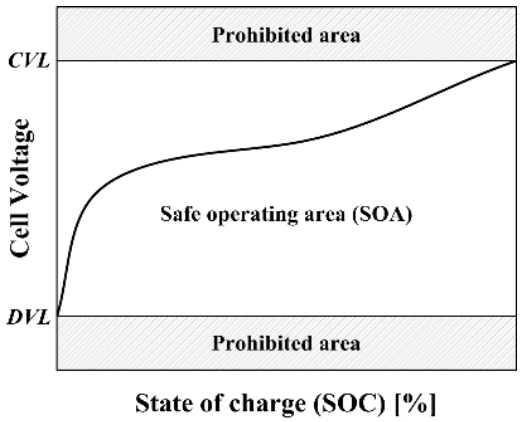

Figure 1. Cell voltage versus state of charge characteristic of the Li-ion battery. Legend: CVL, charging voltage limit; DVL, discharging voltage limit.

This paper presents a new active balancing circuit that uses double energy carriers. The proposed circuit simultaneously implements cell-to-pack and pack-to-cell balancing operations in the same switching period without overlapping. It can therefore effectively equalize batteries during charging and discharging conditions and can achieve fast balancing by using the high balancing power rate of double energy carriers. The structure and operation of the proposed active balancing circuit are proposed in Section 2. Experimental results are presented in Section 3. Discussion and comparison with other balancing circuits are given in Section 4. The conclusion is given in Section 5.

2. Proposed Active Balancing Circuit

2.1. Structure of Proposed Circuit

The proposed balancing circuit (Figure 2) consists of a cell-access network and energy-transfer network. The cell-access network is composed of $n + 1$ bidirectional switches (S_1–S_{n+1}) and four MOSFETs (Q_3–Q_6), where n is the number of serially connected battery cells. This network makes a balancing energy path between unbalanced cells and energy carriers of the energy-transfer network. The energy-transfer network is based on the fly-back converter, and is composed of two MOSFETs (Q_1, Q_2), two diodes (D_1, D_2), and two transformers (T_1, T_2) as energy carriers. T_1 has a turns ratio n:1 for the pack-to-cell balancing operation; T_2 has a turns ratio 1:n for the cell-to-pack balancing operation.

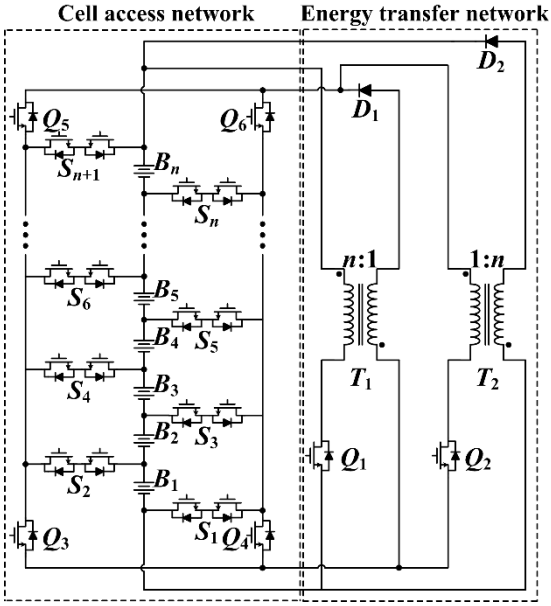

Figure 2. Circuit structure of the proposed active balancing circuit using double energy carriers.

2.2. Principles of Operation

For a single switching period T_s, the proposed circuit simultaneously implements the cell-to-pack and pack-to-cell balancing operations by using T_1 and T_2. The circuit uses a fixed switching frequency $f_s = 1/T_s$ and operates in discontinuous conduction mode (DCM) to achieve zero-current switching (ZCS). The equivalent circuits (Figure 3) and theoretical waveforms (Figure 4) of the two distinct operation modes were obtained under the following assumptions: (1) the pack-to-cell balancing operation transfers the balancing energy from the total battery pack B_P to the most-depleted cell B_N; (2) the cell-to-pack balancing operation transfers the balancing energy from the most-charged cell B_M to B_P; (3) all cells of the battery are constant-voltage sources; and (4) all components are ideal and loss-free.

Mode 1 [t_0–t_1]: At $t = t_0$, switches Q_1, Q_2, S_{BM}, and S_{BM+1} are turned on to collect the energy of B_P to magnetizing inductance L_{m1} and the energy of B_M to magnetizing inductance L_{m2}. In this mode, L_{m1} and L_{m2} simultaneously collect the energy from B_P and B_M. When B_M is an even-parity cell, switches Q_3 and Q_6 of the cell-access network are connected to B_M, and when B_M is an odd-parity cell, Q_4 and Q_5 are connected (Table 1). In this mode, the currents of L_{m1} and L_{m2} increase linearly as:

$$i_{Lm1}(t) = i_{BP}(t) = \frac{V_{BP}}{L_{m1}}(t - t_0), \tag{1}$$

$$i_{Lm2}(t) = i_{BM}(t) = \frac{V_{BM}}{L_{m2}}(t - t_0). \tag{2}$$

Table 1. On-state switches for balancing operations.

Symbol		Pack-to-Cell Operation		Cell-to-Pack Operation	
		Pack to Even	Pack to Odd	Even to Pack	Odd to Pack
Collect (*Mode* 1)	[t_0–t_1]	Q_1	Q_1	Q_2, Q_3, Q_6, S_{BM}, S_{BM+1}	Q_2, Q_4, Q_5, S_{BM}, S_{BM+1}
Release (*Mode* 2)	[t_1–t_2]	Q_3, Q_6, S_{BN}, S_{BN+1}	Q_4, Q_5, S_{BN}, S_{BN+1}	-	-

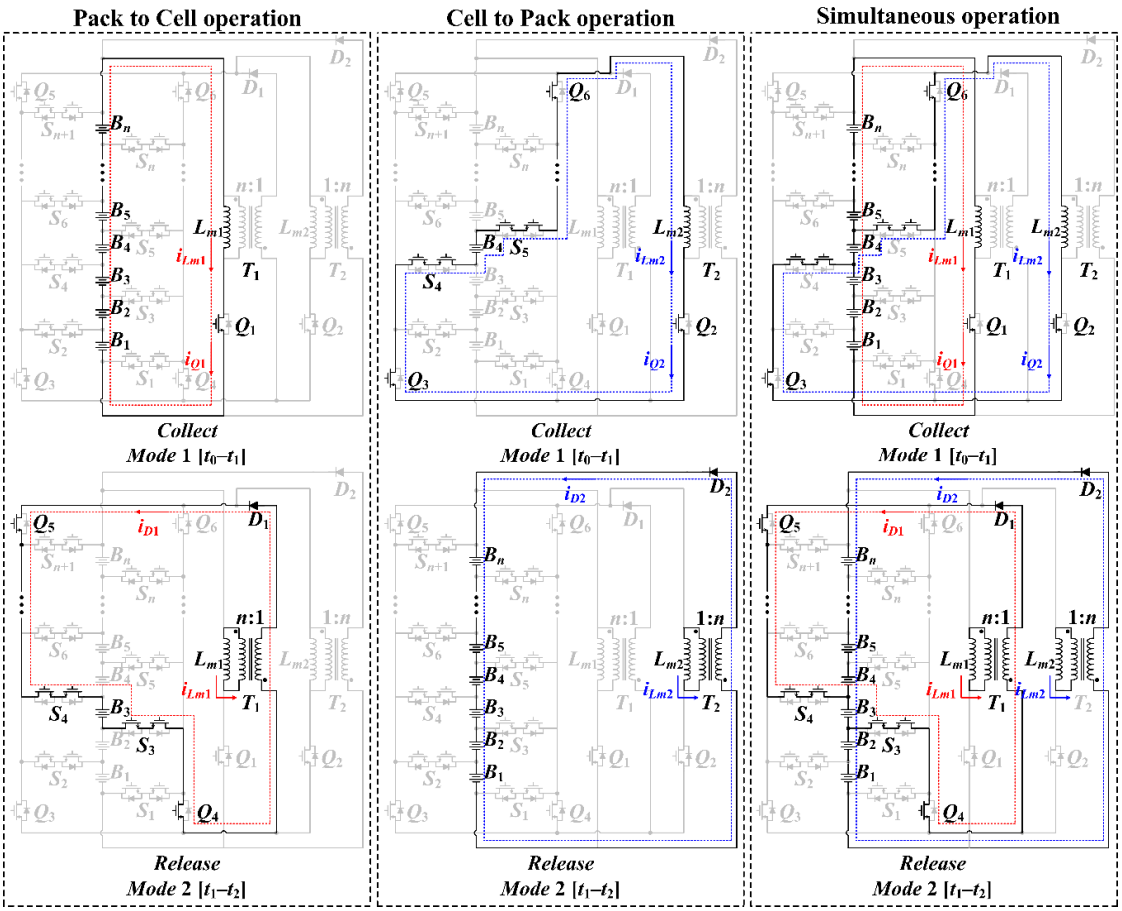

Figure 3. Operation modes for pack-to-odd cell and even cell-to-pack operations.

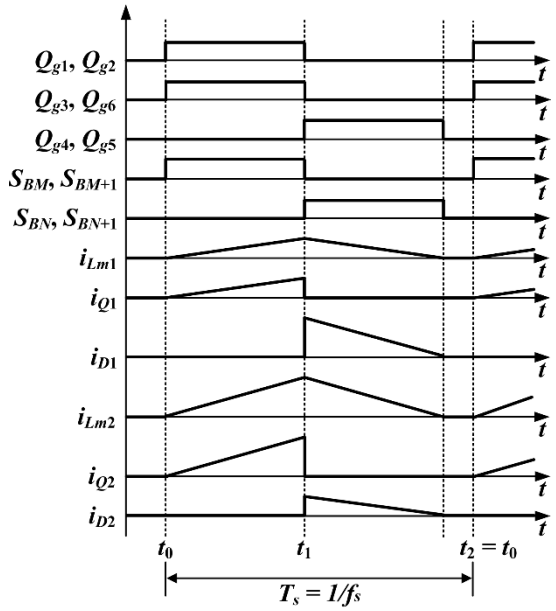

Figure 4. Operation waveforms of proposed active balancing circuit for pack-to-odd cell and even cell-to-pack operations.

Mode 2 [t_1–t_2]: At $t = t_1$, switches Q_1, Q_2, S_{BM}, and S_{BM+1} are turned off and S_{BN}, S_{BN+1}, D_1, and D_2 are turned on to release the energy in L_{m1} and L_{m2} to B_N and B_P, respectively. In this mode, L_{m1} and L_{m2} simultaneously release stored energy to B_N and B_P. When B_N is an even-parity cell, the switches

Q_3 and Q_6 of the cell-access network are turned on; otherwise, Q_4 and Q_5 are turned on (Table 1). In this mode the current of D_1 and D_2 can be expressed as:

$$i_{D1}(t) = i_{BN}(t) = N \cdot i_{Lm1}(t) = \frac{n \cdot V_{BP}}{L_{m1}}(t_1 - t_0) - \frac{n^2 \cdot V_{BN}}{L_{m1}}(t - t_1), \quad (3)$$

$$i_{D2}(t) = i_{BP}(t) = \frac{i_{Lm2}(t)}{n} = \frac{V_{BM}}{n \cdot L_{m2}}(t_1 - t_0) - \frac{V_{BP}}{n^2 \cdot L_{m2}}(t - t_1). \quad (4)$$

This mode is terminated when i_{D1} and i_{D2} decrease to 0 and all switches and diodes are turned off.

2.3. Balancing Algorithm

To implement an effective balancing operation, the balancing algorithm for the proposed circuit is based on a state of charge (SOC). The SOC values of each cell are measured using an equivalent circuit (Figure 5a). R_i is the series resistance, R_d is the diffusion resistance, C_d is the diffusion capacitance and I is the current of the battery cell. These parameters can be measured as in [27], so the SOC can be obtained as

$$V_T = \mathrm{OCV(SOC)} + V_d + V_i \approx \mathrm{OCV(SOC)} + (R_d + R_i) \times I \quad (5)$$

where OCV(SOC) represents the relationship between the SOC and calculated open circuit voltage (OCV), as in Figure 5b.

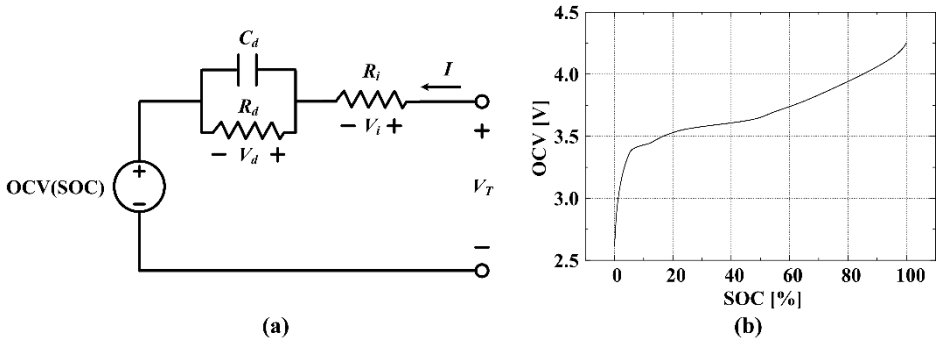

Figure 5. (**a**) Equivalent circuit of the Li-ion battery cell and (**b**) OCV (state of charge (SOC)): OCV versus SOC characteristic of the experimental Li-ion cell.

The balancing algorithm for the proposed balancing circuit consists of four procedures (Figure 6), and this algorithm iterates during every monitoring sampling of the battery pack:

(1) Evaluate the SOC values (SOC_k) of all n serially-connected cells.
(2) Calculate the average SOC value of n cells (SOC_{avg}) and find the SOC values of the strongest cell B_M (SOC_{BM}) and the weakest cell B_N (SOC_{BN}).
(3) If $\mathrm{SOC}_{dev,BM} = \mathrm{SOC}_{BM} - \mathrm{SOC}_{avg} > \mathrm{SOC}_{th}$, then run the cell-to-pack balancing operation, where SOC_{th} is the threshold SOC value to determine whether the balancing operation is performed.
(4) If $\mathrm{SOC}_{dev,BN} = \mathrm{SOC}_{avg} - \mathrm{SOC}_{BN} > \mathrm{SOC}_{th}$, then run the pack-to-cell.
(5) Repeat operations (1)–(3) until $\mathrm{SOC}_{dev,BM} \leq \mathrm{SOC}_{th}$ and $\mathrm{SOC}_{dev,BN} \leq \mathrm{SOC}_{th}$.

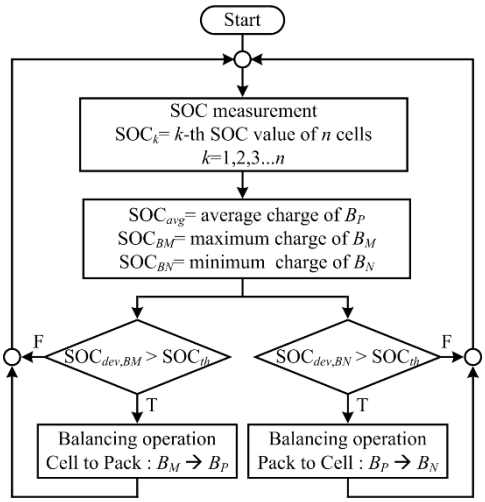

Figure 6. Balancing algorithm for the proposed balancing circuit.

3. Experimental Results

The proposed balancing circuit simultaneously implements pack-to-cell and cell-to-pack balancing operations so the balancing powers of each operation are set as equal. The average balancing powers $P_{b.avg1}$ from the battery pack to the weakest cell and $P_{b.avg2}$ from the strongest cell to the battery pack are

$$P_{b.avg1} = \frac{V_p{}^2 D^2}{2L_{m1} f_s}, \tag{6}$$

$$P_{b.avg2} = \frac{V_{BM}{}^2 D^2}{2L_{m2} f_s}, \tag{7}$$

where D is the duty ratio of both Q_1 and Q_2. Assuming $nV_{BM} = V_P$ and $P_{b.avg1} = P_{b.avg2}$, the ratio of L_{m1} and L_{m2} can be set as

$$L_{m1} = n^2 L_{m2}. \tag{8}$$

When the battery pack is charged or discharged using current I_P, the sum of the balancing current and I_P should not exceed the charging current limit (CCL) or the discharging current limit (DCL):

$$i_{Lm1}(t_1) + i_{Lm2}(t_1) + I_P = i_{D1}(t_1) + i_{D2}(t_1) + I_P < \text{CCL, DCL}. \tag{9}$$

From (1), (2), and (8), L_{m1} and L_{m2} should be designed as

$$L_{m1} = n^2 L_{m2} > \frac{n(n+1)V_{BM}D}{f_s(\text{CCL, DCL} - I_P)}. \tag{10}$$

To verify the effectiveness of the proposed circuit, a prototype (Figure 7) was fabricated and tested. The battery pack was composed of six serially-connected LIB cells (LG Chem., Ltd.) which had a nominal capacity of 4400 mA·h. The battery pack had a nominal voltage of 21.6 V with CCL = 4.3 A and DCL = 6.45 A. The prototype had f_s = 40 kHz and D = 0.5 and turns ratios 1:6 for T_1 and 6:1 for T_2, with designed values of L_{m1} = 1.45 mH and L_{m2} = 39.6 µH from (8) and (10). The switches and diodes were FDS3572 and FSV540 from On Semiconductor Co., Ltd. and the gate drivers were TLP250 from Toshiba Co., Ltd. The voltages of each cell were measured using a PXI-6254 data-acquisition board (National Instruments, Ltd.) and the gate signal for all switches was output by a PXI-6542 digital waveform generator (National Instruments, Ltd.).

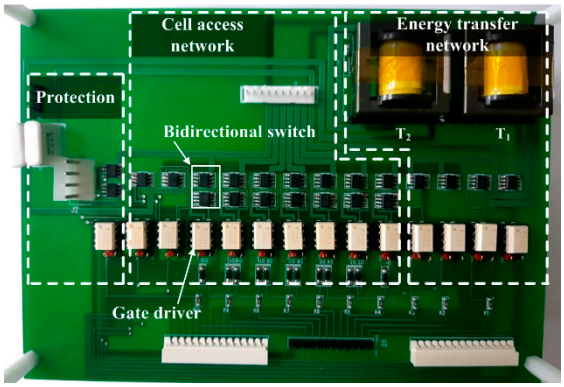

Figure 7. Prototype of the proposed balancing circuit for equalization of six cells.

First, the six cells were balanced to prove the operation of the proposed balancing circuit and balancing algorithm. The voltage and current waveforms (Figure 8) were measured using a 610Zi oscilloscope (Teledyne Co., Ltd.). The waveforms agreed well with the theoretical waveforms (Figure 4). The initial SOC values of the six serially-connected cells were 69.94%, 79.24%, 79.19%, 78.17%, 73.18%, and 75.41%, and the cell numbers were assigned based on the order of series connection in the battery pack; the bottom-located cell was cell number 1 and the top-located cell was cell number 6. SOC_{th} was set to 0.2% and all cells converged to 3.883 ± 0.002 V (SOC = 74% ± 0.2%) after 93 min (Figure 9). This experiment shows that the proposed balancing circuit provides good simultaneous implementation of cell-to-pack and pack-to-cell balancing operations.

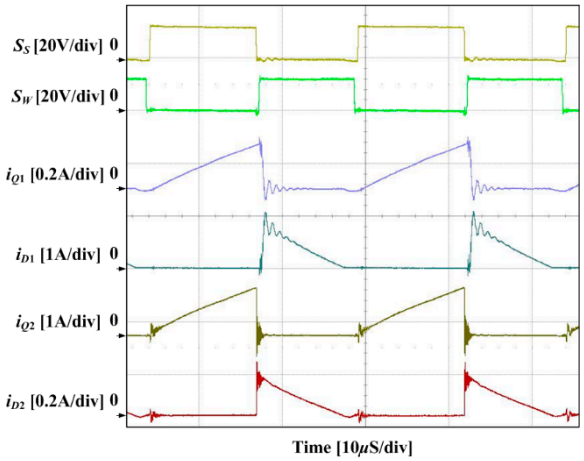

Figure 8. Operational waveforms of the proposed balancing circuit.

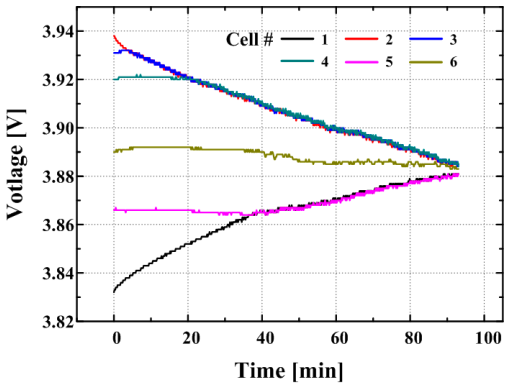

Figure 9. Voltage versus balancing time for the proposed charge equalization; six cells were connected in a static condition.

Second, the balancing operation of the strongest cell was measured within a charging operation (Figure 10) and the speeds of only pack-to-cell and cell-to-pack balancing operations were compared. CVL was set to 3.94 V (SOC = 80%) and the battery pack had charging current I_{ch} = 1.5 A. The strongest cell (cell number 1) was set to 3.577 V (SOC = 30.64%) and the other five cells (cell numbers 2–5) were set to 3.53 V ± 0.01 V (SOC = 20.33% ± 0.02%). The strongest cell reached the CVL after 91.5 min in the pack-to-cell balancing operation (Figure 10a) and after 101.66 min in the cell-to-pack balancing operation (Figure 10b).

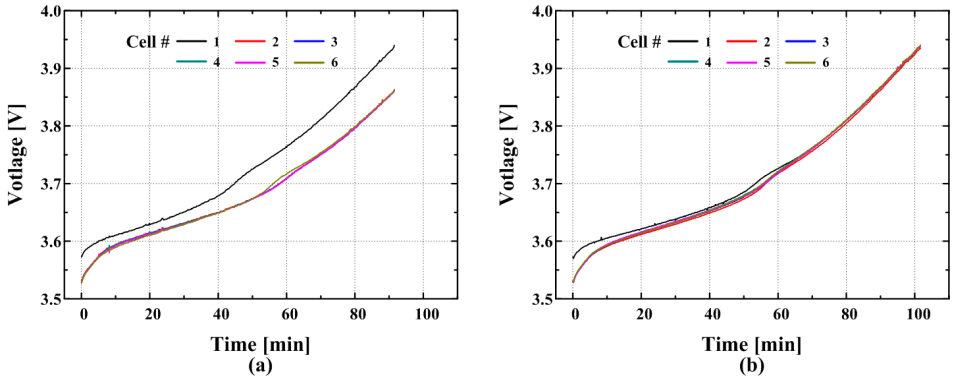

Figure 10. Voltage versus charging time for the battery pack: (**a**) pack-to-cell balancing in charging operation and (**b**) cell-to-pack balancing in charging operation.

Third, the balancing operation of the weakest cell was implemented within a discharging operation (Figure 11) and the speeds of both balancing operations were compared in the same manner. The DVL was set to 3.529 V (SOC = 20.21%) and the battery pack had a discharging current I_{dis} = 1.5 A. The weakest cell (cell number 1) was set to 3.829 V (SOC = 69.68%) and the other five cells (cell numbers 2–5) were set to 3.938 V ± 0.02 V (SOC = 79.81% ± 0.02%). The weakest cell reached the DVL after 83.66 min in the cell-to-pack balancing operation (Figure 11a) and after 90 min in the pack-to-cell balancing operation (Figure 11b).

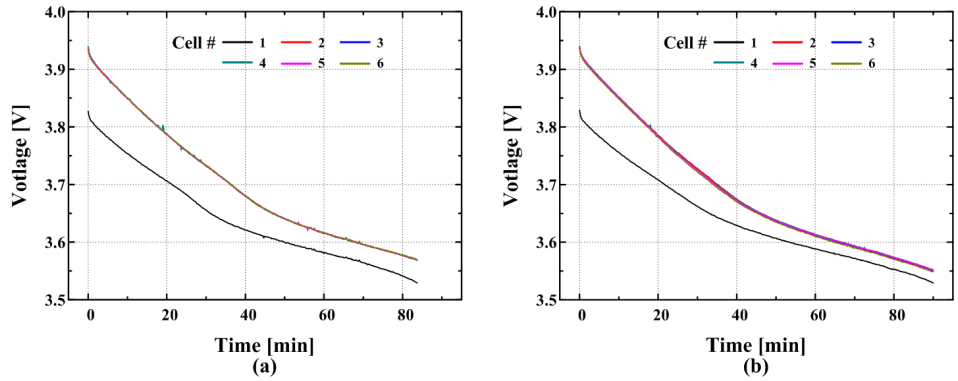

Figure 11. Voltage versus discharging time for the battery pack: (**a**) cell-to-pack balancing in discharging operation and (**b**) pack-to-cell balancing in discharging operation.

These (Figures 10 and 11) show that the cell-to-pack balancing operation has good speed in balancing the strongest cell during a charging operation and that the pack-to-cell balancing operation is suitable for balancing the weakest cell during a discharging operation. These results mean that a simultaneous balancing operation of the proposed circuit can be effectively used in both charging and discharging operations.

Finally, one charging/discharging period (I_{ch} = I_{dis} = 1A) between CVL = 4.061 V (SOC = 90.1%) and DVL = 3.429 V (SOC = 10.13%) was measured for a non-balancing operation and balancing operation (SOC_{th} = 0.2%) (Figure 12). The initial SOCs were 89.22%, 84.89%, 79.92%, 87.8%, 81.78%,

and 82.92%. During the discharging period, the weakest cell reached the DVL at 187.33 min in the non-balancing operation and at 194.16 min in the balancing operation. During the next charging period, the strongest cell reached the CVL at 372.83 min in the non-balancing operation and at 404.83 min in the balancing operation; i.e., one charging/discharging period in the balancing operation was increased by 32 min, which increased the capacity of battery pack by 8.58%. These results mean that a battery pack supported by the proposed balancing circuit can store more energy from the energy sources and supply more energy to the application of the battery pack.

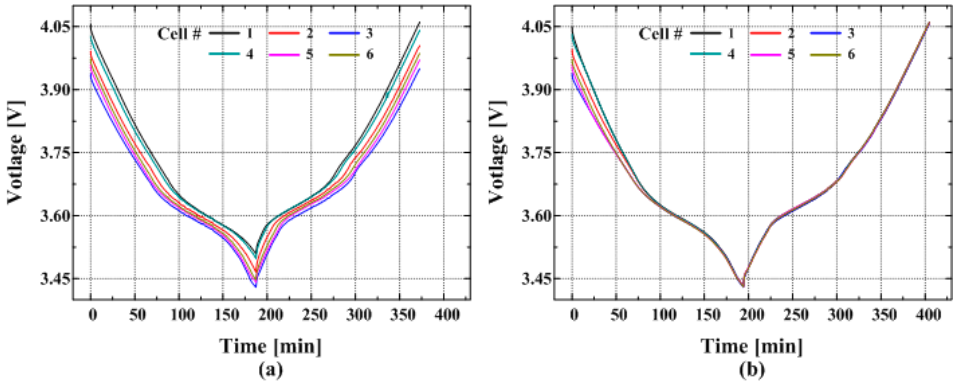

Figure 12. Voltage versus time under the one cyclic discharging/charging period: (**a**) without charge equalization, (**b**) with charge equalization.

4. Discussion

To display the advantages of the proposed circuit we have compared it with previous balancing circuits (Table 2); the number of components in the balancing circuit and balancing performance, including control method and balancing speed, were evaluated under the assumption of n cells per battery pack.

Table 2. Comparison of balancing circuits for n cells battery packs.

		Flyback [8]	Half Bridge [10]	Switched Capacitor [15]	LC Resonant [18]	Buck-Boost [20]	Proposed
Balancing circuit	**Transformer (multi-winding)**	1(2)	1(n + 1)	0	0	1(n/2)	2(4)
	Diode	2n − 1	4n	0	0	0	2
	Inductor	0	1	0	1	0	0
	Capacitor	0	2	n	1	0	0
	MOSFET	2n − 2	2	2n + 4	2n + 10	2n	2n + 8
Balancing performance	**Transfer range**	C to P	P to C	AC	C to C	C to C	P to C and C to P
	Energy carrier	1	1	n	1	1	2
	Balancing speed	Normal	Normal	Slow	Fast	Fast	Fast
	Control method	Hard	Easy	Easy	Hard	Hard	Normal

Legend: P, pack; C, cell, AC, adjacent cell.

When the minimum balancing time was calculated, CCL = 4.3 A and DCL = 6.45 A at $I_{ch} = I_{dis} = 0$. In addition, a six serially-connected battery pack was assumed by using 4400 mA·h Li-ion cells from LG-Chem, Ltd; the total charge Q of the cell was 15,840 C. The SOC values of six serially connected cells were assumed to be 47% (3.633 V, 7444.8 C), 48% (3.638 V, 7603.2 C), 49% (3.644 V, 7761.6 C), 51% (3.66 V, 8078.4 C), 52% (3.669 V, 8236.8 C), and 53% (3.679 V, 8395.2 C). The efficiency of balancing circuit was assumed to be 100%, so Q_b = 7920 C (3.651 V, SOC = 50%).

The time shared flyback balancing circuit used in [8] requires one transformer, 2n − 1 diodes, and 2n − 2 MOSFETs. The primary winding of the transformer is connected to the battery pack through the diode and the secondary winding is connected to a cell through the cell access network. The circuit

measures all cell voltages and then sorts the cell voltages in ascending order. During the half switching period, the transformer sequentially collects the energy of each cell using the cell access network at a current < DCL, except for the weakest cell with the lowest cell voltage. The collected energy is released to the battery pack during the other half of the switching period at a current < DCL/n. Since the energy collection from each cell depends on the cell voltage, the order of cell voltages must be verified for each switching period. This increases the complexity of the balancing algorithm and gate signal control. The time shared flyback balancing circuit only supports the cell-to-pack balancing operation, meaning the weakest cell ($Q_{weakest}$) determines the balancing time and the balancing operation is not efficient under the discharging conditions of the battery pack. Because this circuit uses the transformer as an energy carrier, DCL $\approx (2/D) \cdot i_B$ and $t_B > 2n \cdot (Q_b - Q_{weakest})/(D \cdot \text{DCL})$, where i_B is the average balancing current. Thus, the calculated minimum balancing time is 1,105 s.

The half-bridge balancing circuit used in [10] requires one multi-winding transformer, $4n$ diodes, one inductor, two capacitors, and two MOSFETs. The primary winding of the multi-winding transformer is connected to the battery pack through the half bridge structure and the secondary windings are connected to the battery cells through the full bridge rectifiers. This circuit collects the energy of the battery pack during the half switching period at a current < CCL and releases this energy to the weakest cell during the other half switching period at a current < CCL/n. When the collected energy is released to the weakest cell, the secondary windings are clamped to the cell voltage of the weakest cell. All rectifiers except the weakest cell are off and the balancing energy is delivered only to the weakest cell. The half-bridge balancing circuit does not require cell voltage detection and the balancing algorithm is very simple. The switches operate in fixed duty. Therefore, the circuit is very easy to control. However, since the circuit only supports the pack-to-cell balancing operation, the strongest cell ($Q_{strongest}$) determines the balancing time and the balancing operation is not efficient under the charging condition of the battery pack. Because the circuit uses the transformer as an energy carrier, CCL $\approx (2/D) \cdot i_B$ and $t_B > 2n \cdot (Q_{strongest} - Q_b)/(D \cdot \text{CCL})$; the calculated minimum balancing time is 1,657 s. The half-bridge balancing circuit requires one multi-winding transformer and many diodes, which are the main hurdles to implementing a balancing circuit for high capacity battery packs.

The switched capacitor circuit used in [15] requires n capacitors and $2n + 4$ MOSFETs. Unlike the conventional switched-capacitor circuit of [13], this circuit adds an auxiliary capacitor (C_A) and switches to allow energy transfer between the top cell and the bottom cell, meaning it has a faster balancing speed than a conventional circuit. The balancing energy is transferred by shunting the capacitor from one cell to another adjacent cell alternately; it does not require cell voltage detection. The balancing algorithm is very simple, but the balancing speed is slow when the cell-voltage difference between adjacent cells is small. In this circuit, the capacitor C collects energy when the capacitor voltage V_{cap} is lower than the cell voltage V_{cell}. Otherwise, the capacitor releases energy to the cell; the amount of charge transferred for one switching operation is $Q_t = C \cdot d \left| V_{cell} - V_{cap} \right|$. Because the total deviation of the i-th cell charges Q_i from Q_b is $\sum_{i=1}^{n} |Q_i - Q_b|$, the amount of charge transferred by the circuit per each switching operation is $Q_{t,n} > \left[\sum_{i=1}^{n-1} C_{(i,i+1)} \cdot d \left| V_{cell(i)} - V_{cap(i,i+1)} \right| + C_A \cdot d \left| V_{cell(n)} - V_{cap(A)} \right| \right]$, where $V_{cell(i)}$ is the voltage value of i-th cell, $V_{cap(i,i+1)}$ is the voltage value of capacitor $C_{(i,i+1)}$, which is located between i-th cell and $(i + 1)$-th cell, and $V_{cap(A)}$ is the voltage value of C_A. This circuit transfer $Q_{t,n}$ totals $N = t_B/T_s$ times during the balancing operation of t_B, meaning the total transferred balancing charge $Q_T = Q_{t,n} \times N = \left[\sum_{i=1}^{n-1} C_{(i,i+1)} \cdot \left| V_{cell(i),initial} - V_{cap(i,i+1),fianl} \right| + C_A \cdot \left| V_{cell(n),initial} - V_{cap(A),final} \right| \right]$, where $V_{cell(i),initial}$ is initial voltage of the i-th cell and $V_{cap(i,i+1),final}$ and $V_{cap(A),final}$ are the final voltages of $C_{(i,i+1)}$ and C_A, respectively. Finally, these factors determine t_B as $t_B > \left(\sum_{i=1}^{n} |Q_i - Q_b| \right) / (Q_T / t_B)$ and $t_B > \left[\left(\sum_{i=1}^{n} |Q_i - Q_b| \right) / \left(\sum_{i=1}^{n-1} C_{(i,i+1)} \cdot \left| V_{cell(i),initial} - V_{cap(i,i+1),final} \right| + C_A \cdot \left| V_{cell(n),initial} - V_{cap(A),final} \right| \right) \right]^{1/2}$; the calculated minimum balancing time was 28,586 s at $C_{(i,i+1)} = C_A = 25$ µF, $T_s = 25$ µs, and $V_{cap(i,i+1),final} = V_{cap(A),final} \approx 3.651$ V.

The LC resonant balancing circuit used in [18] requires one inductor, one capacitor, and $2n + 10$ MOSETs. This circuit transfers the balancing energy using the LC resonance, so all MOSFETs operate

with ZCS. In addition, it can achieve a fast balancing speed in a large-scaled battery pack because it directly transfers the collected energy from the strongest cell to the weakest cell. Because this circuit uses an LC resonant circuit as an energy carrier, DCL $\approx \pi \cdot i_B$ and the deviation of cell charges Q_i from Q_b, $\sum_{i=1}^{n}|Q_i - Q_b|/2$, determines t_B as $t_B > \pi \cdot \sum_{i=1}^{n}|Q_i - Q_b|/(2 \cdot \mathrm{CCL})$. Thus, the calculated minimum balancing time is 694 s. However, this circuit requires a complex zero-current detection circuit for the control of the gate signal and initializing circuit for the gate driver. In addition, it requires a complex procedure to generate the gate signals, taking into account the target charge states, the SOCs of all cells, the efficiency of the balancing circuit, and the average balancing power.

The buck-boost balancing circuit used in [20] requires one multi-winding transformer and $2n$ MOSFETs. Compared to the buck-boost balancing circuit used in [16], this circuit uses a multi-winding transformer to reduce the number of inductors and to extend the energy transfer range. In the circuit used in [16], the energy transfer is possible only between adjacent cells, but energy transfer between all cells of the battery pack is possible in the circuit used in [20]. Since energy transfer from the strongest cell to the weakest cell is possible, the circuit used in [20] can achieve a fast balancing speed. Because this circuit uses the transformer as an energy carrier, CCL $\approx (2/D) \cdot i_B$ and the deviation of cell charges Q_i from Q_b, $\sum_{i=1}^{n}|Q_i - Q_b|/2$, determines t_B as $t_B > 2 \cdot \sum_{i=1}^{n}|Q_i - Q_b|/\mathrm{CCL}$ for $D = 0.5$; the calculated minimum balancing time is 884 s. The fabrication of a multi-winding transformer is a major hurdle to implementing a balancing circuit for high capacity battery packs. The circuit used in [20] examines the parity between the strongest and weakest cells and works differently for three different parity conditions. Case 1: The circuit operates as a buck-boost converter when the balancing energy is transferred from an odd-numbered cell to an adjacent even-numbered cell. Case 2: The circuit operates as a flyback converter when the balancing energy is transferred from a nonadjacent odd-numbered cell to an even-numbered cell. Case 3: When the balancing energy is transferred between same parity cells, the circuit works like a buck-boost converter to collect the balancing energy and like a fly-back converter to release the collected energy. Thus, the circuit used in [20] requires a very complicated control algorithm.

Compared to the previous balancing circuits, the proposed circuit requires only two transformers, two diodes, and $2n + 8$ MOSFETs. The proposed circuit allows both pack-to-cell and cell-to-pack balancing operations to be used at the same time and requires only two operation modes: the collect mode and the release mode (Figures 3 and 4). The proposed circuit works like a flyback converter for all parity conditions in the strongest and weakest cells and has a faster balancing speed than the circuits used in [18,20]. The proposed circuit collects the energy from strongest cell with $i_B \approx (D/2) \cdot \mathrm{DCL}$ and releases the collected energy to the weakest cell with $i_B \approx (D/2) \cdot \mathrm{CCL}$. Thus, t_B is determined as $t_B > \sum_{i=1}^{n}|Q_i - Q_b|/(D \cdot \mathrm{CCL})$ for CCL < DCL and $D = 0.8$; the calculated minimum balancing time is 552 s, which is the fastest time when compared with other methods. The balancing speed was improved by using double energy carriers and by increasing the switching duty D.

5. Conclusions

In this work, a new active balancing circuit has been proposed. The circuit consists of a cell-access network and an energy-transfer network; these networks are composed of two transformers as energy carriers, two diodes, and $2n + 8$ MOSFETs. The proposed circuit simultaneously performs cell-to-pack and pack-to-cell balancing operations during a single switching period. Thus, a high power rate and fast balancing operation can be achieved. A prototype of the balancing circuit for six Li-ion cells was verified under various experimental conditions. All results show that the proposed circuit can implement an effective balancing operation during when both charging and discharging. A comparison with previous balancing circuits demonstrates that the proposed circuit is well suited for balancing the battery pack.

Author Contributions: S.-W.L. developed the circuit, constructed the hardware prototype, and conducted the experiments. Y.-G.C. supported the experiments and analyzed the experimental results. B.K. provided guidance and key suggestions for this study.

Funding: This research received no-external funding.

Acknowledgments: This research was supported by the Ministry of Science and ICT (MSIT), Korea, under the "ICT Consilience Creative program" (IITP-2019-2011-1-00783), supervised by the Institute for Information and Communications Technology Promotion (IITP).

Conflicts of Interest: The authors declare no conflict of interest.

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