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Solid-phase epitaxy of amorphous Si using single-crystalline Si nanowire seed templates

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We report solid-phase epitaxy of amorphous Si (*a*-Si) shells using crystalline Si (*c*-Si) nanowire cores as seed templates. The *c*-Si core/*a*-Si shell nanowire heterostructures were *in situ* synthesized via a two-step chemical vapor deposition: the Au-catalytic decomposition of SiH_4 for the core *c*-Si nanowires and the subsequent homogeneous decomposition of SiH_4 at higher temperatures for the *a*-Si shells. Upon thermal annealing above 600 °C, the *a*-Si shells crystallize into *c*-Si shells from *c*-Si core nanowires in an epitaxial fashion. We discuss the crystallization kinetics of *a*-Si shells within the frame of Gibbs-Thomson effects arising from the finite size of nanowire seeds. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2817601]

Crystallization of amorphous Si (*a*-Si) thin films at low temperatures has received extensive interest for their attractive applications into Si thin film transistors and Si solar cells.[1–6] In this regard, a number of growth processes to achieve large-grained polycrystalline Si (poly-Si) thin films have been developed including excimer laser annealing and metal-induced crystallization. Crystallization of amorphous Si using the local nucleation seeds is also an interesting scheme, because it can offer advantageous solid-phase crystallization at the controlled sites at low temperatures.[7–10] Relevant growth approaches, reported so far, employ various kinds of nucleation seeds followed by appropriate thermal annealing, including crystalline Si (*c*-Si) layers in contact to *a*-Si layers,[7,8] *c*-Si nanoparticles embedded in *a*-Si layer,[9] and metal nanocrystals embedded in *a*-Si layers.[10] In fact, these synthetic methods have produced large-grained poly-Si at low crystallization temperatures below 600 °C, and reported the improved mobility thin-film transistors. Nevertheless they sometimes display some drawbacks such as mechanical-stress induced damages, randomly oriented grains, and metal contaminations. Single-crystalline Si nanowires, in this respect, can serve as interesting nucleation seeds when imbedded in *a*-Si for its solid-phase crystallization, because their specific crystal orientations in the one-dimensional structures can impose the preferred crystal orientation on the crystallizing *a*-Si matrices upon the subsequent solid-phase crystallization. In addition, provided that the vertical or parallel alignment of single-crystalline Si nanowires is avaialble,[11–13] such ordered nanowire array can offer the promising seed templates for large-area crystallization with preferred crystal orientations. Here, we report the basic characteristics of the solid-phase crystallization of *a*-Si shells surrounding single-crystalline Si nanowires upon thermal annealing. Specifically, we examined the microstructural evolution and the crystallization kinetics of *a*-Si shells around 20 nm thick *c*-Si nanowire cores by extensive transmission electron microscopy study, and compared them with the cases of planar *a*-Si layers on Si wafers reported in literature. We found that the *a*-Si shells crystallize into *c*-Si shells in excellent epitaxial relations with single-crystalline nanowire cores upon thermal annealing. We also discuss the kinetics of crystallization of *a*-Si shells based on our observations within the frame of Gibbs-Thomson effect, arising from the finite size effects of nanowire seed templates.

The *c*-Si core/*a*-Si shell nanowire heterostructures were *in situ* synthesized using a two-step chemical vapor deposition (CVD) using SiH_4 precursors. Figure 1(a) shows the schematics of our syntheses of the nanowire *a*-Si shell/*c*-Si core heterostuctures. First, single-crystalline Si nanowires were grown by the Au catalyst-assisted chemical vapor process.[14,15] Au catalysts of the nanometer scale were prepared by the dispersion of colloidal Au particles of 20 nm in diameter on SiO_2/Si (100), and were subsequently loaded in a quartz tube furnace. The catalytic decomposition of SiH_4 onto Au catalysts occurs at 500 °C and results in the axial growth of single-crystalline Si nanowires. Subsequently, we promote the radial growth of *a*-Si surrounding upon the pregrown Si nanowires by the homogeneous SiH_4 decomposition at the elevated temperature of 550 °C. That is, the axial nanowire growth by the catalytic decomposition of SiH_4 at 500 °C is kinetically facilitated over the radial growth of *a*-Si shell which is only activated above 550 °C. Thus, we were able to grow *c*-Si core/*a*-Si shell nanowire heterostructures by exploiting two different SiH_4 decomposition behaviors at each temperature regime.

We then investigated crystallization behaviors of *a*-Si shell layers by thermal annealing of the *c*-Si core/*a*-Si shell nanowire heterostructures under N_2 flowing at 500, 600, and 800 °C for a given period of time. High-resolution transmission electron microscopy (HRTEM) was employed to observe the epitaxial characteristics at the interfaces between *a*-Si shells and *c*-Si nanowire cores. We found that the majority of Si nanowires in this study grow in the [211] direction along the nanowire direction, and some Si nanowires also grow in the [110] direction. Figure 1(b) shows the typical TEM image of *c*-Si core/*a*-Si shell nanowire heterostructures by the two-step CVD growth, and demonstrates that the core is indeed single crystalline and the shell is amorphous.

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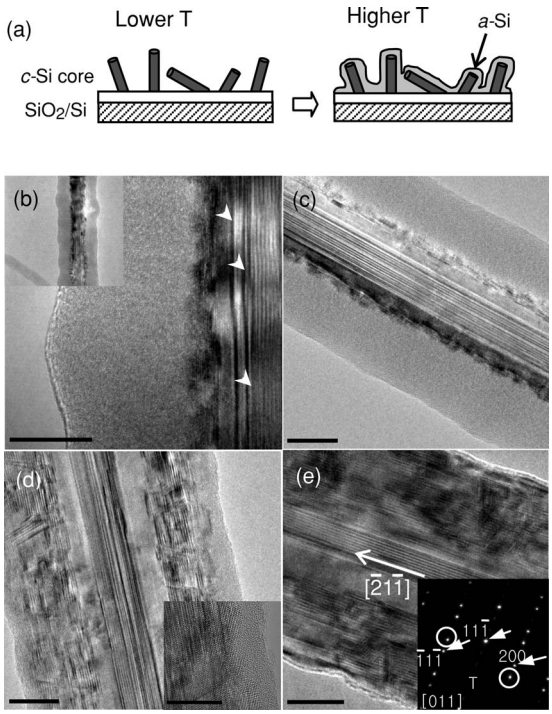

FIG. 1. (a) The growth schematic showing the successive two-step growth of *c*-Si core/*a*-Si shell nanowire heterostructures. [(b)–(e)] Representative HRTEM images of nanowire heterostructures at different annealing temperatures (the scale bar is 20 nm). (b) the as-deposited nanowires consist of amorphous Si shells surrounding crystalline Si cores. The inset shows a lower magnification image. The structural evolutions of nanowire heterostructures upon thermal annealing at (c) 500 °C for 90 min, (d) 600 °C for 30 min, and (e) 800 °C for 30 min. The scale bar of the inset of (d) is 10 nm. The diffraction pattern in the inset of (e) represents twins in the fully crystallized nanowires.

We note the presence of stacking faults parallel to the nanowire axis as marked with white arrows, and they persist after the thermal annealing, as shown in Figs. 1(c)–1(e). These stacking faults are rarely observed in catalytically grown Si nanowires,[14,15] and in our study, we have observed the presence of such unusual dislocations only after the *a*-Si shell deposition at higher temperatures. We do not understand their formation mechanism at the moment; nevertheless, we argue that the presence of these stacking faults does not affect our main conclusions on the crystallization of *a*-Si shells. Figures 1(c)–1(e) show the sequential crystallization behaviors of *a*-Si shell as the N_2 annealing temperature for 30 min increases from 500 to 600 and 800 °C. After annealing at 500 °C, we have not observed any noticeable structural changes, as seen in Fig. 1(c), even for the extended annealing up to 90 min. On the other hand, after annealing at 600 °C, we observed that *c*-Si nanowire core extended its volume outward to the surface, with the presence of only a very thin *a*-Si layer at the outermost surface, as in Fig. 1(d). Evidently, the *a*-Si shells crystallize into *c*-Si shells from the *c*-Si core seed templates upon annealing at above 600 °C. Upon annealing at the higher temperature of 800 °C, the crystallization of *a*-Si shell is completed, as shown in Fig. 1(e). Here, we emphasize that the crystallographic orientation of the crystallizing *a*-Si shell epitaxially templates the orientation of *c*-Si cores; i.e., the crystallization of *a*-Si shell progresses by a layer-by-layer growth fashion. Indeed, the diffraction pattern in the inset of Fig. 1(e) demonstrates that the fully crystallized nanowires at 800 °C, as a whole core-shell nanowire, are single crystalline only with few twins

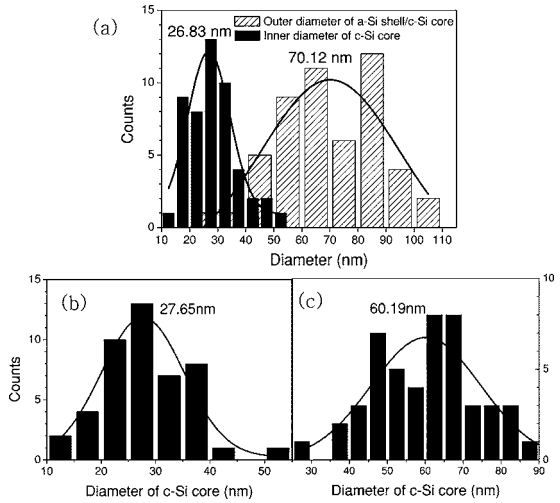

FIG. 2. Histograms of *c*-Si core diameter distributions measured from *a*-Si shell/*c*-Si core heterostructures (a) as it is deposited, (b) annealed at 500 °C for 90 min, and (c) annealed at 600 °C for 30 min. The histogram filled with declined lines in (a) shows the outer diameter distribution of *a*-Si shell/*c*-Si core structures. The smooth curves are Gaussian fits.

present. The differences are, nevertheless, observed with HRTEM images. The crystallized shell layers contains additional structural defects such as grains, twins with {111} twin planes, and supercell structures originated from the unstable phase which are often observed in defective structures. Additional stacking faults in the shell are sometimes in the ⟨111⟩ directions, interruption in the stacking sequence of close-packed planes, both along the growth direction and the radial direction.

Having identified that the crystallization of *a*-Si shells proceeds in a layer-by-layer fashion by solid-phase epitaxy (SPE), we then investigated its kinetic characteristics by extensive TEM analyses. Due to the intrinsic diameter distribution of *c*-Si nanowires, we examined 50 samples at each annealing temperature by TEM and we extracted the SPE rates from the statistical distribution. Figure 2(a) is the histogram of the diameter distribution obtained from the as-deposited nanowire heterostructures, as shown in Fig. 1(b). The average diameter of *c*-Si nanowire core is measured to be 27 nm, which is reasonably consistent with the size of Au colloidal particles of 20 nm, and the average outer diameter of nanowire heterostructures is 70.12 nm. Figure 2(b) shows that the diameter of crystalline core remains almost the same as 27.62 nm upon annealing at 500 °C for 90 min. After annealing at 600 °C for 30 min, it increases to 60.19 nm, as shown in Fig. 1(d), followed by a complete crystallization at the 800 °C annealing. Based on the determined values above, the growth rate of *a*-Si layers on *c*-Si nanowires is calculated to be 4.6×10^{-2} and 5.6 Å/min at 500 and 600 °C, respectively. These values of growth rate are indicated as solid squares in an Arrhenius plot as in Fig. 3, along with the SPE rates of *a*-Si layer deposited under the various conditions on flat *c*-Si substrates from literature for comparison. In particular, the SPE rates of vacuum evaporated *a*-Si layer are indicated as dotted line in Fig. 3. We found that the value of the SPE growth rate of *a*-Si shells on *c*-Si nanowire core in our experiment is smaller by two orders of magnitudes than the case of *a*-Si layers on planar *c*-Si.

The smaller SPE growth rate of *a*-Si are often attributed to an effect of oxygen inevitably incorporated in *a*-Si. Oxygen has been known to sensitively inhibit the crystallization

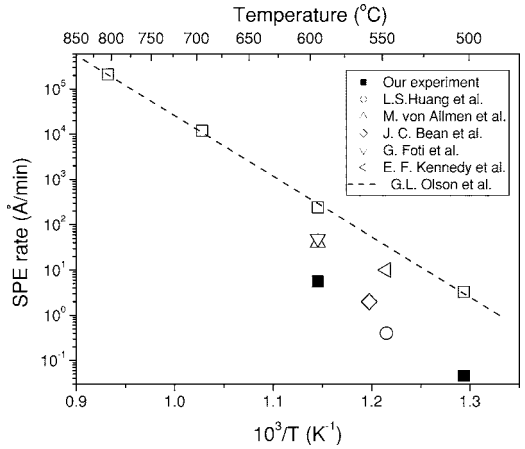

FIG. 3. Temperature dependence of the SPE growth velocity in amorphous Si shell deposited on *c*-Si nanowires (■), compared with those of others' (○) evaporated amorphous Si, where the columnar epitaxial growth occurs upon annealing at 550 °C (by Huang *et al.*), (△) evaporated amorphous Si upon annealing at 600 °C (by von Allmen *et al.*), (◇) surface of amorphous Si after air exposure (by Bean and Poate), (▽) amorphous Si layer containing oxygen content of $5\times10^{20}/\mathrm{cm}^3$ (by Foti *et al.*), (◁) amorphous Si layers in which oxygen with $2.5\times10^{20}/\mathrm{cm}^3$ is ion implanted (by Kennedy *et al.*), and (…) amorphous Si deposited by vacuum evaporation.

of *a*-Si, leading to much lower SPE growth rates of *a*-Si layers. The presence of oxygen in high contents also causes a columnar growth if the amount of oxygen within the amorphous layer exceeds some values.[1,2] For instance, Huang *et al.* have reported that *a*-Si layer deposited on Si wafers which is cleaned by HF dipping followed by a H_2O rinse contained about 2×10^{20} oxygen atoms/cm^3 and accordingly showed the columnar epitaxial growth.[1] In our two-step CVD growth, the oxygen content is presumed to be small, and its amount within *a*-Si shells can be estimated to be an order of $\sim10^{19}/\mathrm{cm}^3$ according to Ref. 16, where a similar deposition method with ours was employed.[16] Nevertheless, the SPE rate of nanowire heterostructures in our study displays the smallest value despite the presumed low oxygen content. Moreover, the epitaxial growth of *a*-Si layer surrounding Si nanowire is observed to occur in a layer-by-layer fashion but not in a columnar epitaxial growth. Thus, the lower SPE growth rate of nanowire heterostructures in our study cannot be attributed to the oxygen impurities within the *a*-Si shells.

The lower SPE rate in our experiments can arise from the small size of *c*-Si nanowires used as the seed templates for the crystallization of *a*-Si. According to the thermally activated growth theory,[17] the solid-phase growth velocity ν is given by

$$\nu = kT/h \cdot \delta \exp(-E_a/kT)[1-\exp(-\Delta g_{ca}/kT)],$$

$$\approx \Delta g_{ca}/h \cdot \delta \exp(-E_a/kT) \quad \text{when } \Delta g_{ca} < kT, \tag{1}$$

where δ is the distance across the interface of crystalline and amorphous phases, E_a is the activation energy for the crystallization, and Δg_{ca} is the free energy difference between crystalline and amorphous phases. Here, E_a is usually interpreted as the energy involved in bond breaking or bond arrangement responsible for SPE growth, and it can be obtained from the slope of the plot in Fig. 3. When looking into our results in Fig. 3, although the numbers of data are not sufficient to fit a linear line, the activation energy seems to be not so different from that of the vacuum evaporated films measured by Olson and Roth.[6] Equation (1) also indicates that the SPE growth velocity is proportional to the free energy difference between the crystalline and amorphous phase Δg_{ca}. According to Gibbs-Thomson effects,[18] the free energy of nanosized particle of phase α faced with phase β is raised by an amount of $2\gamma V_m/r$, where γ is α/β the interfacial energy, V_m is the molar volume of β, and the r is the radius of the nanosized particle. We argue that this size effect can be applied to our study where the *c*-Si nanowire core possesses the diameter of 20 nm, leading to a larger free energy than that of a flat Si substrate. As a result, the free energy difference between the crystalline and amorphous phase Δg_{ca} becomes smaller when *c*-Si nanowires are employed as the seed templates for the crystallization of *a*-Si, and the SPE growth velocity is decelerated according to Eq. (1).

In summary, we investigated the SPE growth behavior of *a*-Si layers when *c*-Si nanowires are employed as the seed templates. It was found that the *a*-Si shells crystallize from the interface between the *a*-Si shell and *c*-Si core in a layer-by-layer epitaxy by thermal annealing at the relatively low temperatures. The measured SPE growth rate is lower compared with that of amorphous Si layers on flat Si substrates, and we attributed this to the size effects arising from the nanosized diameters of the template *c*-Si nanowires. Based on our observations, we suggest that the array of Si nanowires can be a promising seed template for the SPE to achieve a highly textured poly-Si thin film by imposing a preferred orientation of *c*-Si nanowires upon the crystallizing *a*-Si layers.

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